

# SPECIFICATION

Electronic Version 1.2.8

Stylesheet Version 1.0

## HIGH PERFORMANCE VERTICAL PNP TRANSISTOR AND METHOD

### Background of the Invention

[0001] Technical Field

[0002] The present invention relates to a high performance PNP transistor and method of forming vertical PNP and NPN transistors.

[0003] Related Art

[0004] The ever increasing use of mobile communications is driving improvements in radio frequency (RF) communications. In particular, this expanding market is demanding lower power consumption and increased performance. One possible solution that has found many applications is bipolar complementary metal-oxide semiconductor (BiCMOS) technology. See e.g., Wilson, et al., "Process HJ: A 30 GHz NPN and 20 GHz PNP Complementary Bipolar Process for High Linearity RF Circuits," BCTM, 1998, page 164; Onai, et al., "Self-Aligned Complementary Bipolar Technology for Low-Power Dissipation and Ultra-High Speed LSI's," IEEE TED, 43:3, 1995, page 413; Miwa et al., "A Complementary Bipolar Technology for Low Cost and High Performance Mixed Analog/Digital Applications," BCTM, 1996, page 185; and Chyan et al., "A 50 GHz 0.25um . . . BiCMOS Technology for Low-Power Wireless-Communication VLSI's," BCTM, 1998, page 128.

[0005] One problem with increasing usage of this technology, however, is that only high performance vertical NPN transistors are currently available. Current low performance lateral PNP transistors are only available with a cutoff threshold (f<sub>T</sub>) of less than 1 GHz.

[0006] In view of the foregoing, there is a need in the art for a high performance PNP

transistor and a method for creating NPN and PNP transistors that both exhibit high performance.

## Summary of the Invention

[0007] The invention includes a method and resulting structure for fabricating high performance vertical NPN and PNP transistors. The resulting high performance vertical PNP transistor includes an emitter region including silicon and germanium, and with the emitter sharing a single layer of silicon with the base of the NPN transistor. The method adds two additional masking steps to conventional fabrication processes for CMOS and bipolar devices, thus representing minor additions to the entire process flow. The resulting structure significantly enhances PNP device performance.

[0008] A first aspect of the invention is directed to a vertical PNP transistor comprising: an emitter region including silicon and germanium.

[0009] A second aspect of the invention is directed to vertical PNP and NPN transistors comprising: a single layer of silicon that forms an emitter region of the PNP transistor, an extrinsic base region of the NPN transistor and an intrinsic base region of the NPN transistor.

[0010] A third aspect of the invention is directed to a method of forming a PNP transistor while forming a CMOS device and an NPN transistor using at least two masking steps in addition to masking steps utilized in forming the CMOS and NPN devices, the method comprising: a first masking step that defines a first opening through which implants for an intrinsic base and a collector of the PNP transistor are made; and a second masking step that defines an emitter of the PNP transistor.

[0011] The foregoing and other features of the invention will be apparent from the following more particular description of embodiments of the invention.

## Brief Description of the Drawings

[0012] The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

[0013]

FIG. 1 show a first step of a method for fabricating a high performance PNP

device;

- [0014] FIGS. 2 and 3 show a second and third step, respectively, of the method;
- [0015] FIG. 4 shows an optional fourth step of the method;
- [0016] FIGS. 5-15 show respective fifth to fifteenth steps of the method; and
- [0017] FIG. 16 shows a sixteenth step of the method and the resulting high performance NPN and PNP transistors.

## Detailed Description of the Invention

- [0018] The invention includes a method and resulting structure for fabricating high performance vertical NPN and PNP transistors. The method generates a high performance vertical PNP transistor as part of conventional SiGe BiCMOS fabrication technology. The resulting high performance vertical PNP transistor includes an emitter region including silicon and germanium, and has its emitter sharing a single layer of silicon with the NPN transistor's base. This structure is the result of application of a SiGe low temperature epitaxial layer that forms polysilicon over the PNP region and mono-crystalline and poly-crystalline silicon over the NPN region, followed by a single implant that forms the extrinsic base of the vertical NPN and emitter of the vertical PNP. The method adds two additional masking steps to conventional SiGe fabrication processes for CMOS and bipolar devices, thus representing minor additions to the entire process flow.

- [0019] With reference to the accompanying drawings, FIGS. 1-16 illustrate fabrication process steps. Throughout the drawings, an NPN region 2 in which a vertical NPN transistor will be created is shown on the left, and a PNP region 4 in which a vertical PNP transistor will be created is shown on the right. It should be recognized that some of the steps of fabrication according to conventional SiGe technology have been omitted for brevity and clarity. Further, it should be understood that some of the conventional SiGe technology fabrication steps have been illustrated for clarity, but these steps do not necessarily form a part of the invention.

- [0020] In a first step, shown in FIG. 1, a first masking step is provided in which a photoresist 10 is applied, e.g., by spin coating, onto a silicon dioxide layer 22

(hereinafter "oxide"). Photoresist 10, and any other photoresist used herein, may be any well known or later developed photoresist material. An opening 14 is formed in photoresist 10 in a known fashion (e.g., expose and develop) for implantations 15. A first implantation may include an n-type material for creating n-type isolations 23 to p-type substrate 12 if it is desired to isolate the device from substrate 12 and/or existing processing is not provided which achieves the same purpose. Accordingly, this first implantation is optional. Second, a p-type material for creating a collector 16 of the vertical PNP transistor is provided. Finally, an n-type material for creating an intrinsic base 18 of the vertical PNP transistor. A number of other structures may also be created prior to the above-described implantations. Among these structures, as shown in FIG. 1, are shallow trench isolations (STIs) 21, oxide layer 22, and an NPN subcollector 25. The n-type material used here, and throughout this description, may be any well known or later developed material for such doping, e.g., arsenic, phosphorous, antimony, or a combination of these materials. Similarly, the p-type material used here, and throughout this description, may be any well known or later developed material for such doping, e.g., boron, indium, or a combination of these materials. Subsequently, photoresist 10 is removed in a known fashion, e.g., by etching.

[0021] FIG. 2 shows a second step in which a layer of silicon nitride 24 (hereinafter "nitride") is deposited followed by a layer of oxide 26. Bipolar areas are masked with resist 27 and layers 24, 26 etched to reveal non-bipolar areas. The resist 27 is then removed, and layers 24, 26 protect the bipolar areas from CMOS processing. It should be recognized, however, that these steps may not be necessary depending on the CMOS processes. Note, that the figures that follow show layers 24, 26 as though they were not etched. At this point, well known fabrication steps (not shown) to partially generate CMOS devices may be carried out. The CMOS processing may, or may not, leave a blanket nitride film (not shown). CMOS processing, however, removes oxide layer 26, so another oxide layer 26 may need to be re-deposited to protect CMOS areas during bipolar processing.

[0022] FIG. 3 shows a third step in which a second mask is formed by applying a photoresist 28 upon layers 24, 26, and creating an opening 30, e.g., by developing through photoresist 28 and etching layers 22, 24, 26, to expose a surface 31 of oxide

layer 22 (substrate 12) in PNP region 4. Photoresist 28 is then removed, e.g., by etching.

[0023] Turning to FIG. 4, an optional fourth step is illustrated. This optional fourth masking step includes applying a photoresist 32 and developing openings 34 over locations in which an extrinsic base 36 of PNP region 4 will be generated. Next, implantation of an n-type material to form extrinsic base 36 of PNP region 4 may be carried out. Subsequently, photoresist 32 is removed. If this step is not carried out, as shown in FIG. 15, the n-type implant that forms extrinsic base 36 of PNP region 4 can be completed at the end of processing, discussed below, using the NFET source/drain implantation. This latter option saves a masking step but creates higher base resistance and thus lower PNP transistor performance. For clarity, FIG. 5-14 do not show the extrinsic base portions 36.

[0024] FIG. 5 shows a fifth step in which a layer of polysilicon 38 is deposited, which fills the opening over PNP region 4 and touches surface 31. Polysilicon layer 38 may be no less than 10 nm and no more than 100 nm, and is typically approximately 45 nm.

[0025] Next, as shown in FIG. 6, an opening 40 is generated over NPN region 2 by depositing an oxide (not shown) and masking by applying/developing a photoresist (not shown), and etching polysilicon layer 38 to nitride layer 24 over NPN region 2. (Note: oxide may not be necessary depending on prior processing.) At this point, an implantation of N-type material is made to form an NPN collector 50 (this implant may not be necessary depending on prior NPN collector processing). Subsequently, the resist is removed, and etching is conducted to oxide layer 22 or substrate 12 over NPN region 2 depending on subsequent processing.

[0026] In the next step, shown in FIG. 7, an epitaxial layer 42 of silicon-germanium (SiGe) is grown over the entire wafer. As the epitaxial layer 42 grows, the SiGe grows as a mono-crystal layer 44 over NPN region 2 since it is in contact with silicon, but grows a poly-crystalline layer 46 over polysilicon 38, i.e., the area over the PNP region 4. As the deposition occurs, p-type material will be added such that the resulting layer 42 includes a p-type base 48 of NPN region 2. In some cases, epitaxial layer 42 may also include some carbon deposited in proximity to the p-type material added to layer 42. The resulting layer 42 includes a region of germanium with a maximum concentration

of no less than 10% and no more than 30% of the combined silicon and germanium composition.

[0027] FIGS. 8-16 show continuing steps of well known SiGe technology that ultimately result in the final high performance NPN and PNP transistors. These steps are outlined in U.S. Patent No. 5,111,271, hereby incorporated by reference. It should be recognized that these steps may vary somewhat as the integration scheme is adapted to different applications. FIG. 8 shows a step in which an oxide layer 52 is grown over the entire wafer, followed by deposition of a nitride layer 54 and finally a polysilicon layer 56.

[0028] FIG. 9 shows a next step in which another layer of nitride (not shown) is deposited and then etched away to form a mandrel 58 over NPN region 2. In addition, oxide spacers 60 are formed in a conventional fashion (e.g., deposit oxide and etch) adjacent to mandrel 58. Next, a p-type material 61 (e.g., boron) is implanted to form an extrinsic base 62 of NPN region 2 and an emitter 64 of PNP region 2. The p-type material diffuses slowly in mono-crystal layer 44, but diffuses rapidly in the polycrystalline layers, i.e., polysilicon layer 38 and SiGe layer 46. A p-type out-diffusion 65 is formed by the rapid diffusion in polysilicon. As a result, an emitter 64 of PNP region 4 is simultaneously formed with extrinsic base 62 of NPN region 2. The resulting structure includes polysilicon in emitter region 64 of the PNP transistor and mono-crystal silicon in a portion of the extrinsic base region 62 and mono-crystal silicon in the intrinsic base region 63 of the NPN transistor.

[0029] As shown in FIG. 10, the next step involves etching away spacers 60 (FIG. 9) from mandrel 58 and conducting a heavy oxidation 68. As the oxidation occurs, polysilicon layer 56 (FIG. 9) turns to oxide layer 70. However, a portion 71 of polysilicon layer 56 under nitride mandrel 58 remains polysilicon, hence, transferring mandrel 58 shape to the polysilicon layer 56. The resulting structure allows the yet-to-be formed emitter of NPN region 2 to self-align with extrinsic base 62 of NPN region 2.

[0030] Referring to FIG. 11, the next step includes selectively etching away polysilicon portion 71, nitride mandrel 58 and the portion of oxide layer 70, nitride layer 54 and oxide layer 52 thereunder.

[0031] The next step, shown in FIG. 12, includes depositing a polysilicon layer 72 and doping it either during deposition or by implant 74 with an n-type material to form an emitter 76 of NPN region 2.

[0032] As shown in FIG. 13, a nitride layer 78 is deposited. NPN emitter 76 is then masked off with photoresist (not shown). Next, the various layers, i.e., nitride layer 78, polysilicon layer 72, oxide layers 52, 70 and nitride layer 54, are otherwise removed, e.g., by etching. Subsequently, the resist (not shown) is removed.

[0033] The next step, shown in FIG. 14 includes masking NPN region 2 and PNP emitter 64 with photoresist (not shown), and etching the SiGe polysilicon layer 46 and polysilicon layer 38 away. This etch defines the base of NPN transistor 100 and emitter 64 of PNP transistor 102. The photoresist (not shown) is then stripped and oxide layer 26 is etched.

[0034] Referring to FIG. 15, if the optional third mask, shown in FIG. 4, was omitted, the CMOS NFET source/drain processing (not shown) could be used to form extrinsic base 36 of PNP region 4. In this situation, nitride layer 24 (if present ) would be etched, a photoresist mask formed and an N-type material 80 implanted to create extrinsic base 36. The photoresist (not shown) would then be stripped.

[0035] Finally, as shown in FIG. 16, a p-type material 82 implant for forming a PFET source/drain (not shown) is made through a mask (not shown). This implant also forms a PNP collector contact 84.

[0036] With continuing reference to FIG. 16, the resulting vertical transistors 100, 102 include a polysilicon emitter 64 for PNP transistor 102 and a polysilicon emitter 76 for NPN transistor 100. Vertical PNP transistor 102 includes an emitter region 64 including silicon and germanium. In addition, vertical NPN and PNP transistors 100, 102 include a single layer of silicon that forms emitter region 64 of PNP transistor 102, an extrinsic base 62 of NPN transistor 100, and an intrinsic base 63 of NPN transistor 100. The resulting structure provides a PNP transistor 102 with significantly enhanced performance (perhaps having a cutoff frequency  $f_T > 1$  GHz) compared to current lateral PNP transistors.

[0037] The method of forming PNP transistor 102, as described above, uses two

additional masking steps, FIG. 1 and FIG. 3, in addition to masking steps utilized in forming the CMOS devices (not shown) and NPN transistor 102. CMOS process steps not shown may include gate oxide growth, FET polysilicon deposition and etch, spacer growths and/or depositions and etches, extension and halo masks and implants, source/drain masks and implants, etc. The first masking step of FIG. 1 defines an opening 14 through which both PNP intrinsic base 18, PNP collector 16 and PNP n-type isolation 23 (latter, optional if prior mask and implant could be used for same function) implants are made. The second masking step of FIG. 3 defines an opening 30 through which PNP emitter 64 is formed.

[0038] While this invention has been described in conjunction with the specific embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims.